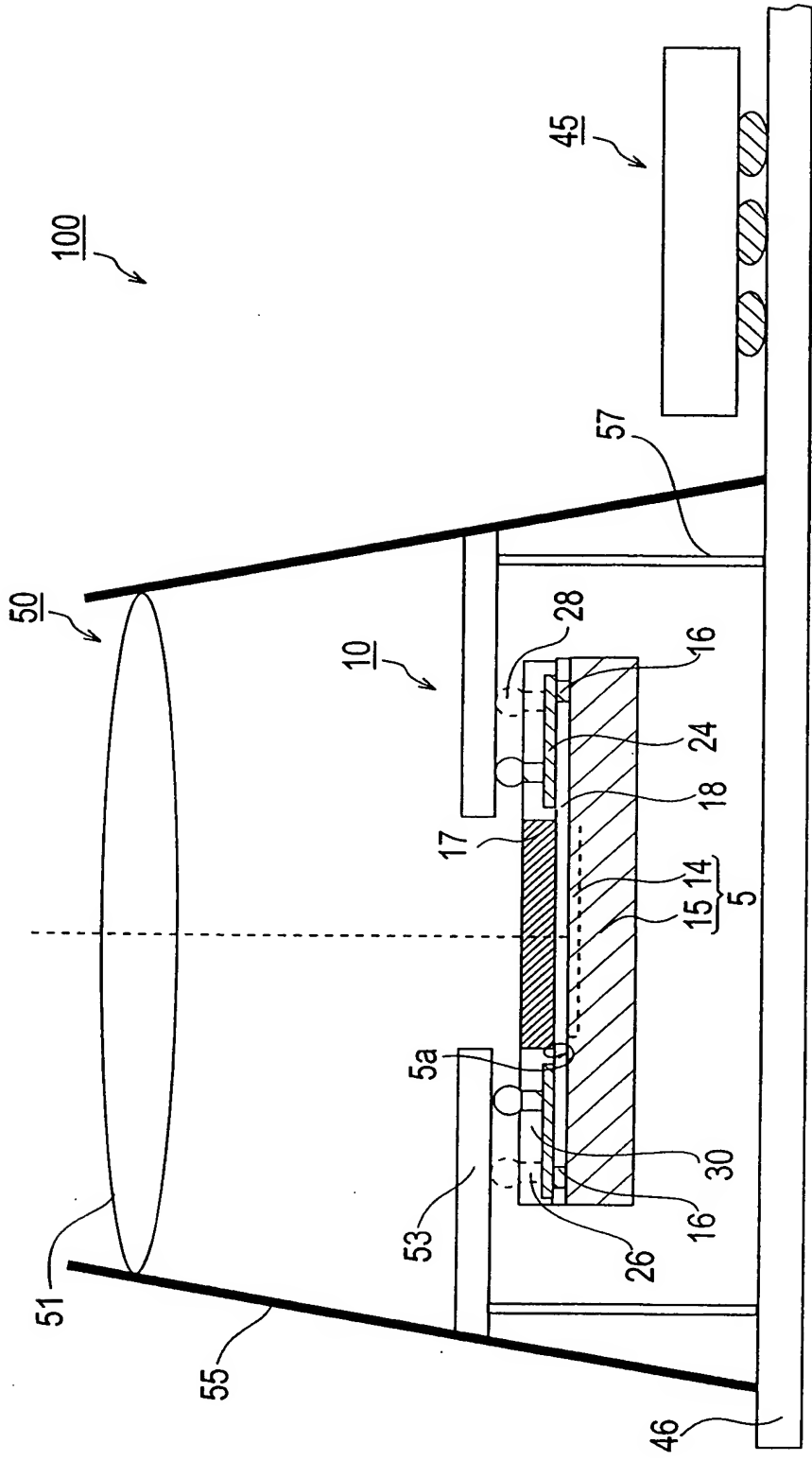
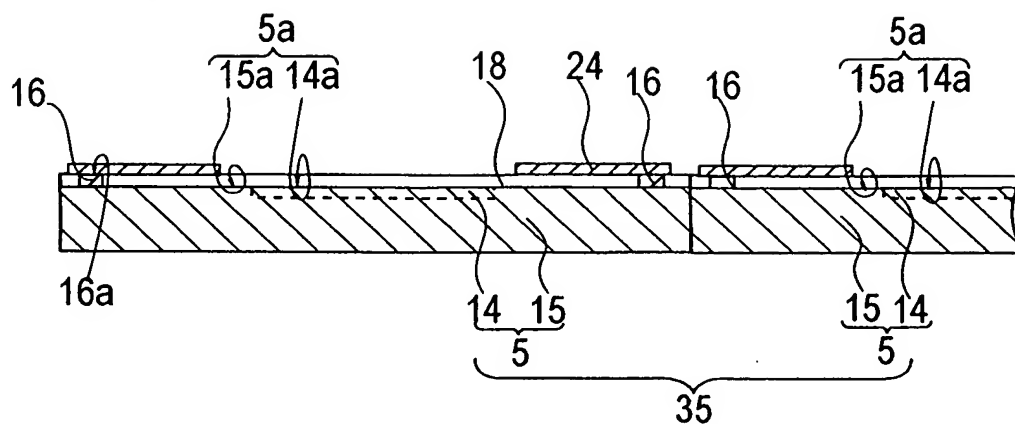


FIG. 1

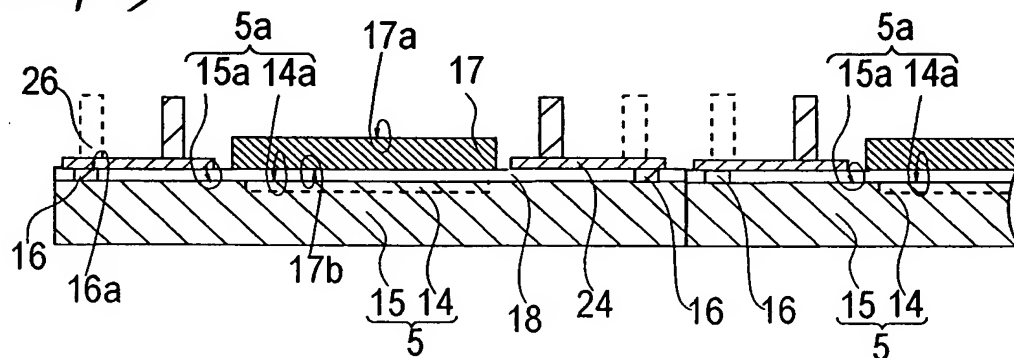




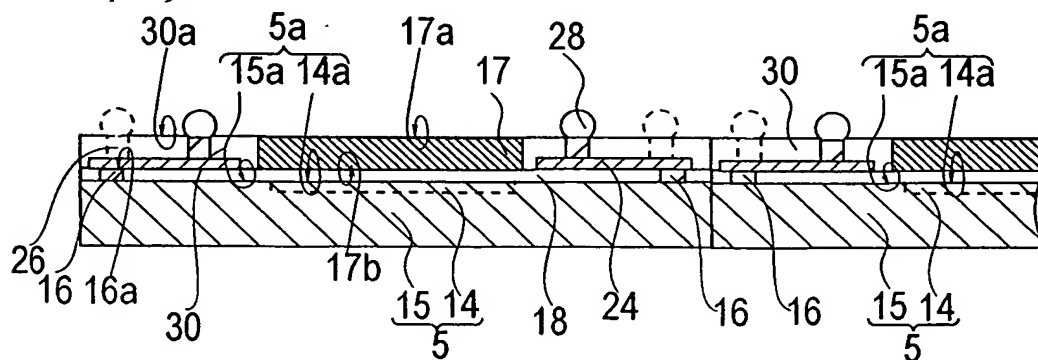
*FIG. 3(A)*



*FIG. 3(B)*



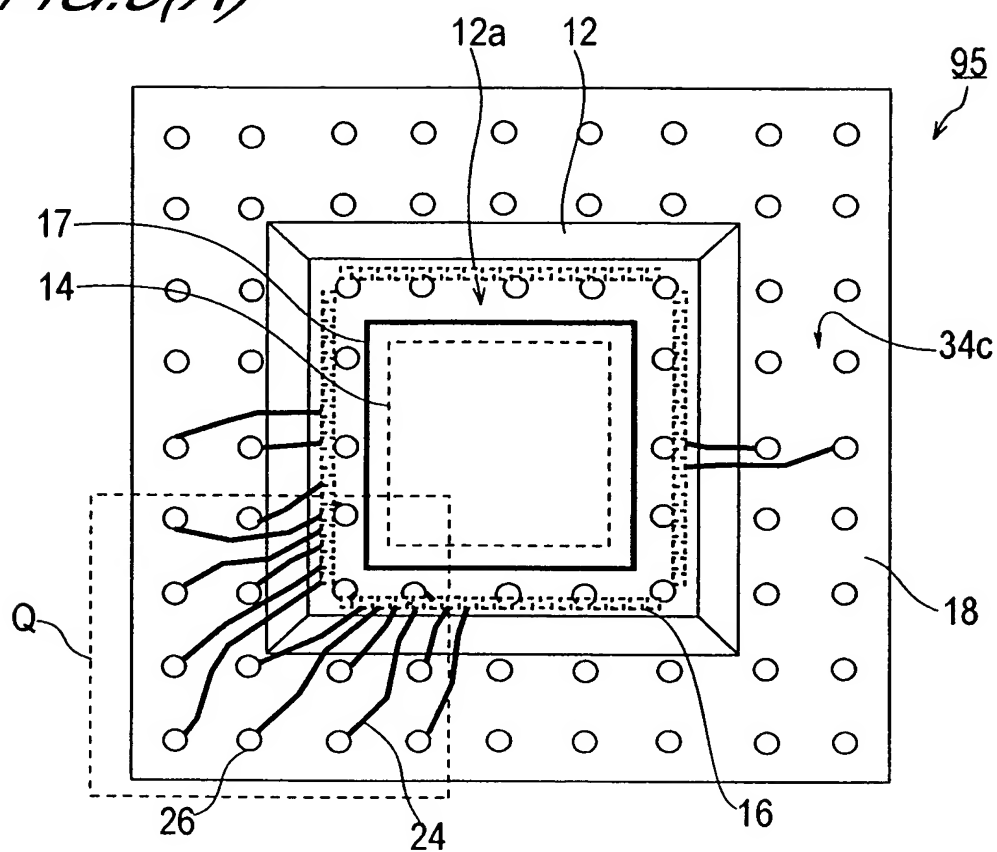
*FIG. 3(C)*



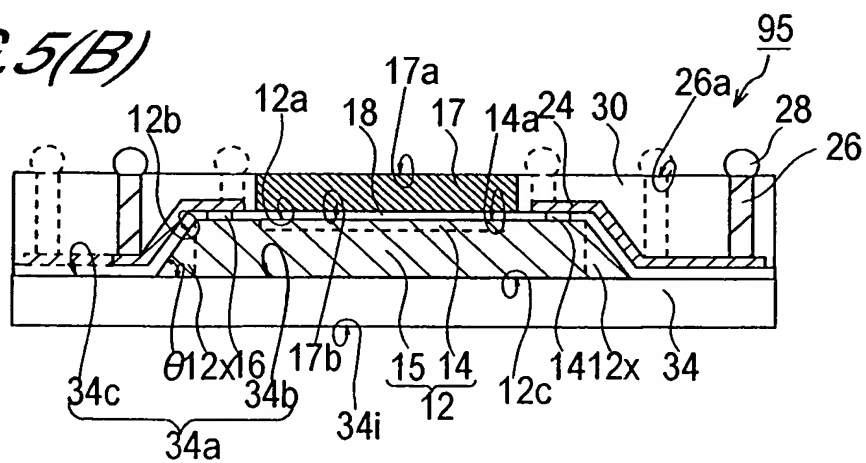
[illegible]

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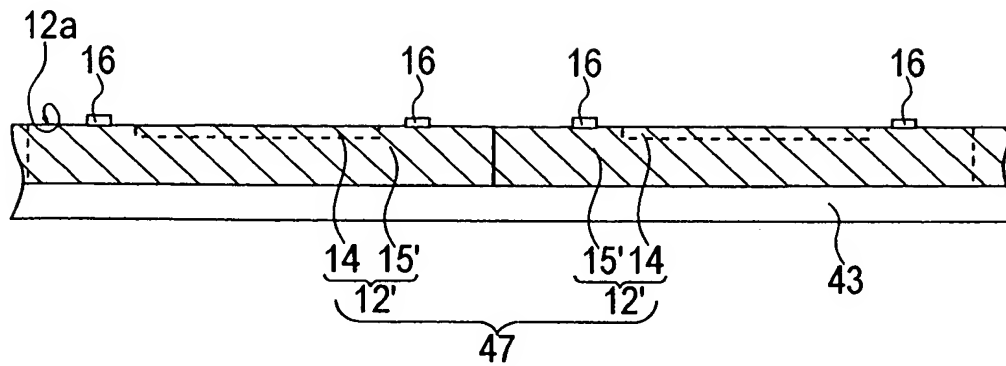
*FIG. 5(A)*



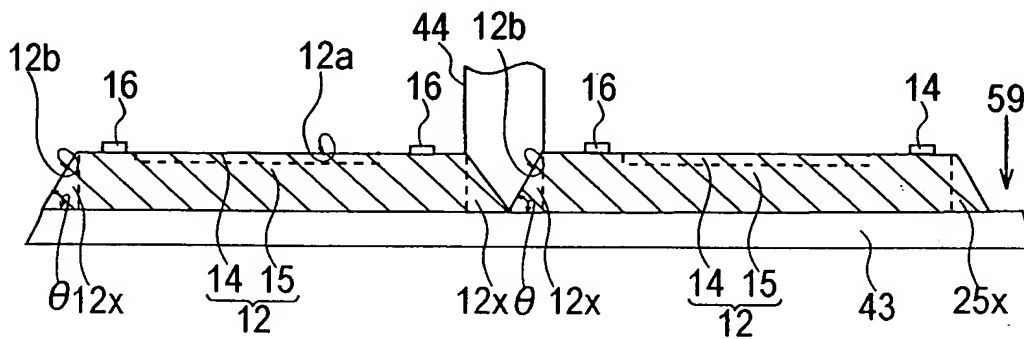
*FIG. 5(B)*



*FIG. 6(A)*



*FIG. 6(B)*



*FIG. 6(C)*

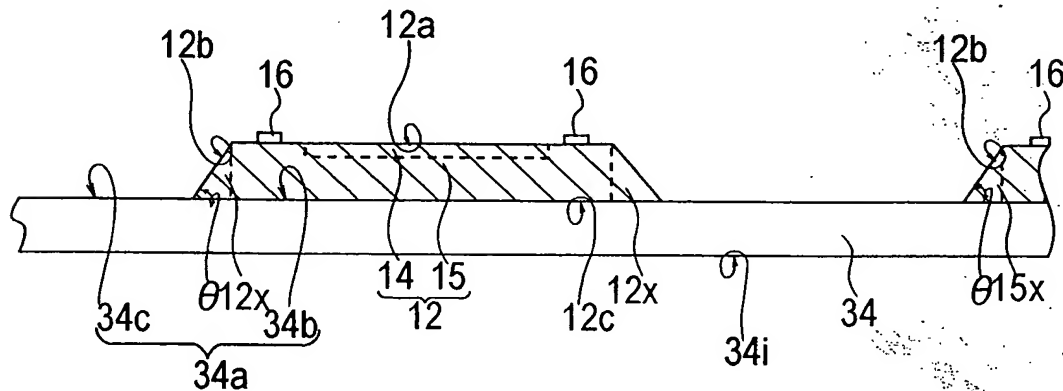








FIG. 9(A)

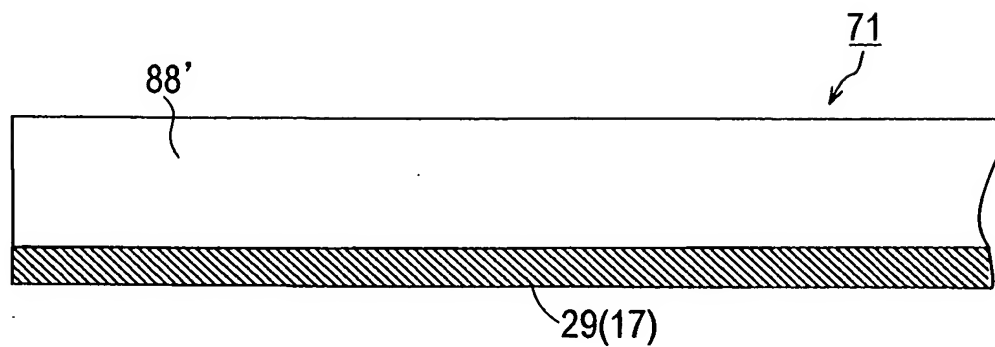


FIG. 9(B)

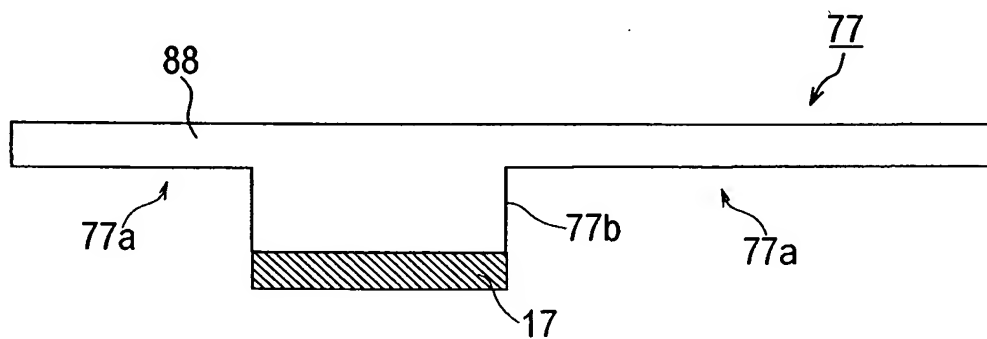


FIG. 9(C)

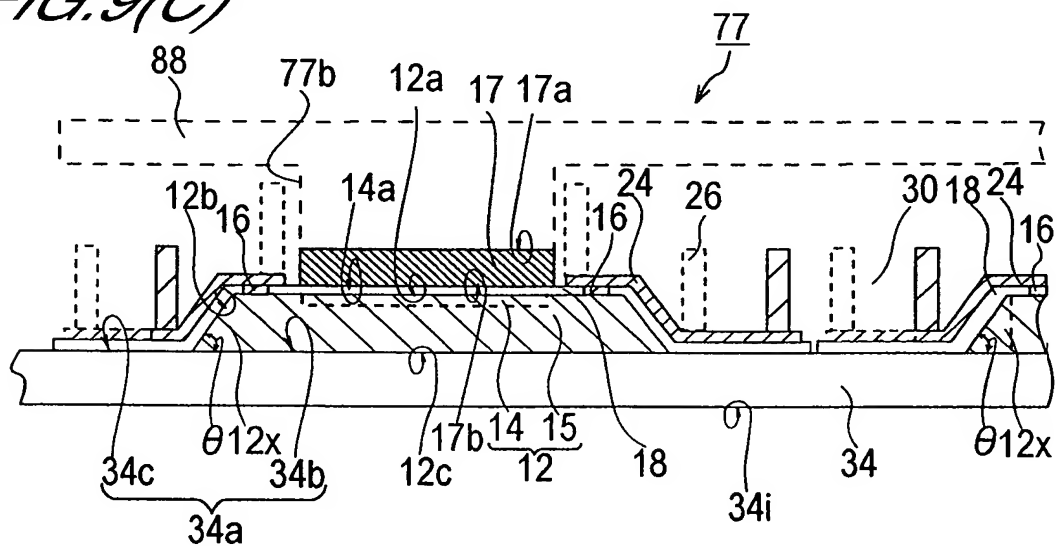
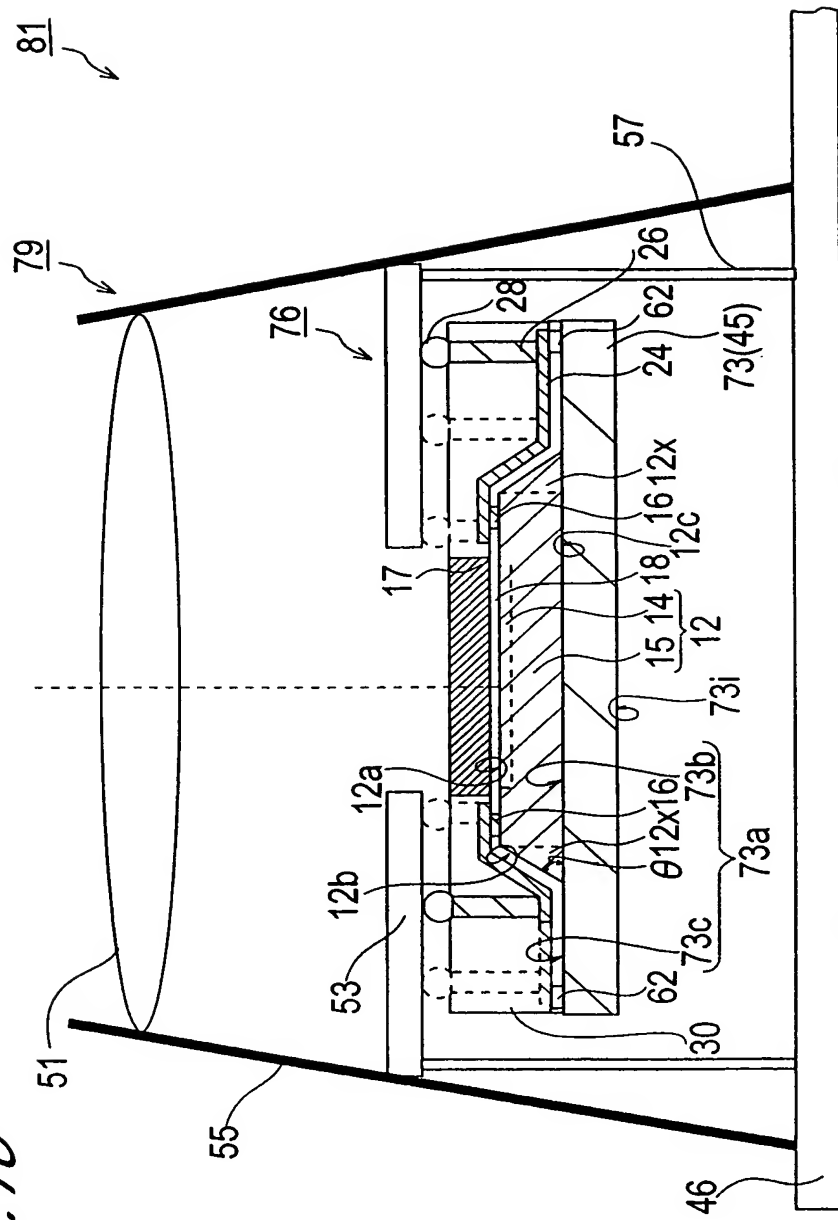
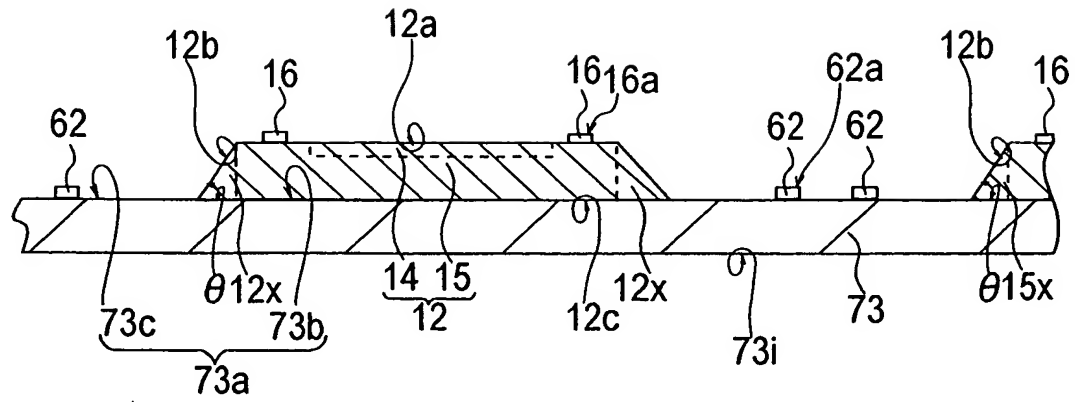


FIG. 10

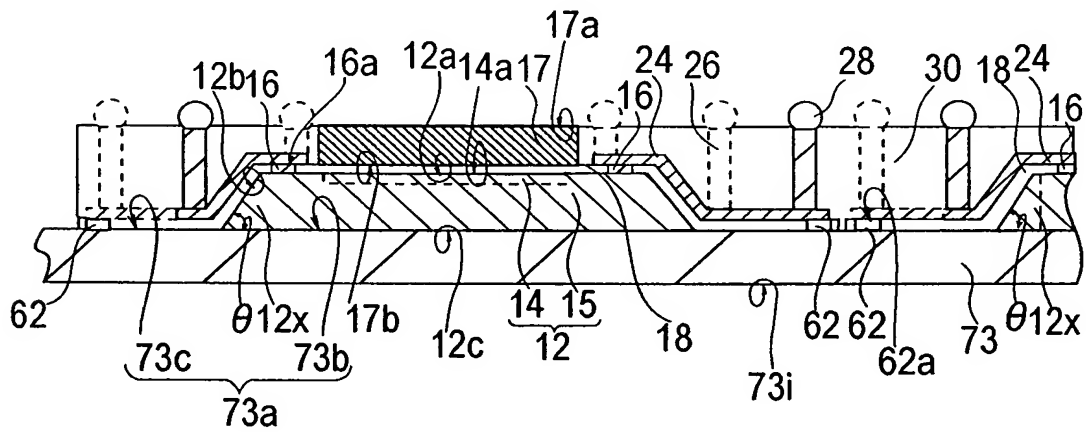


*FIG. 11(A)*

FIG. 12(A)

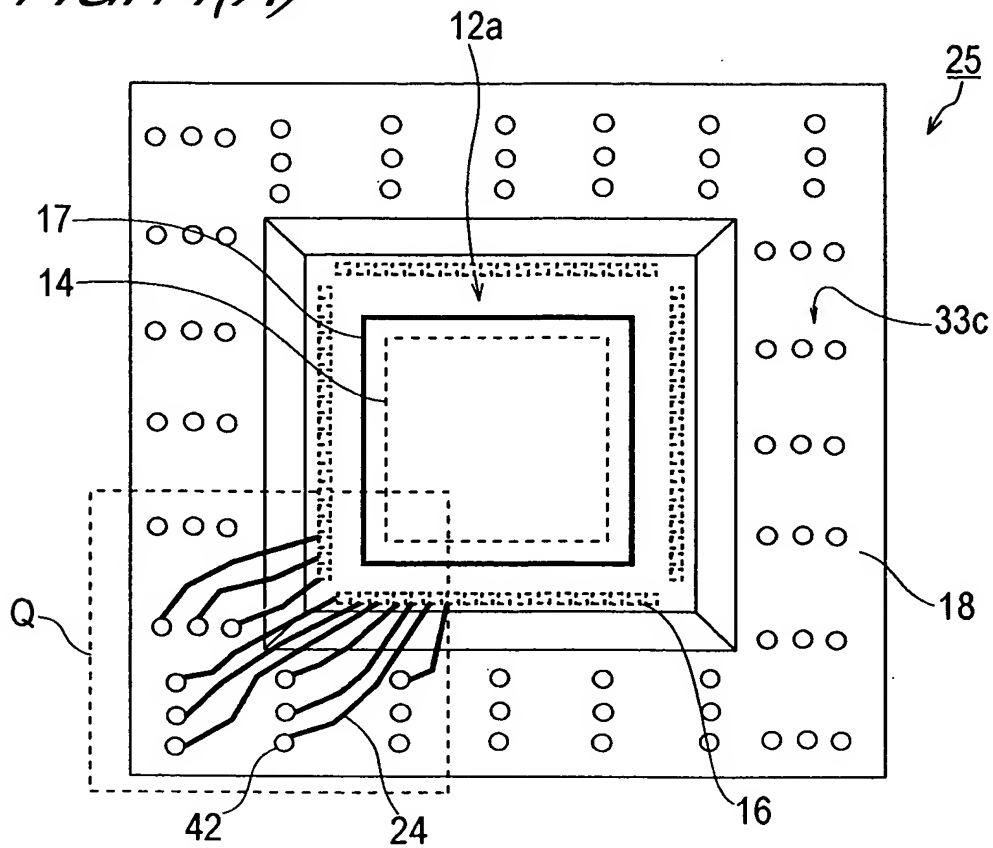


*FIG. 12(B)*

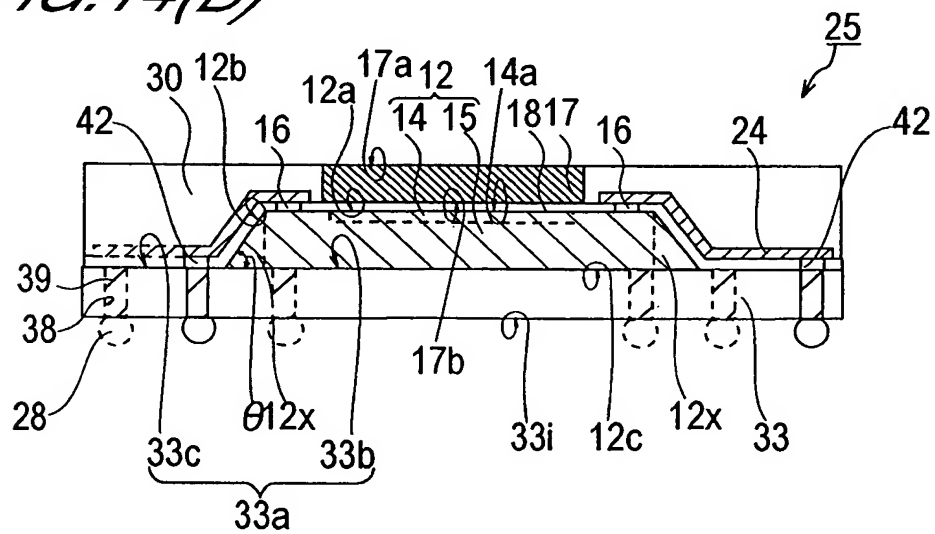




*FIG. 14(A)*

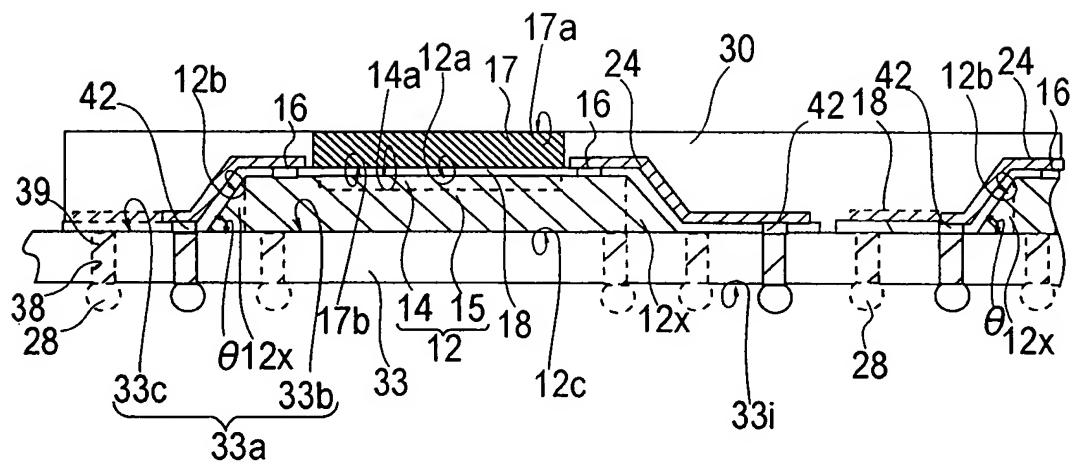


*FIG. 14(B)*

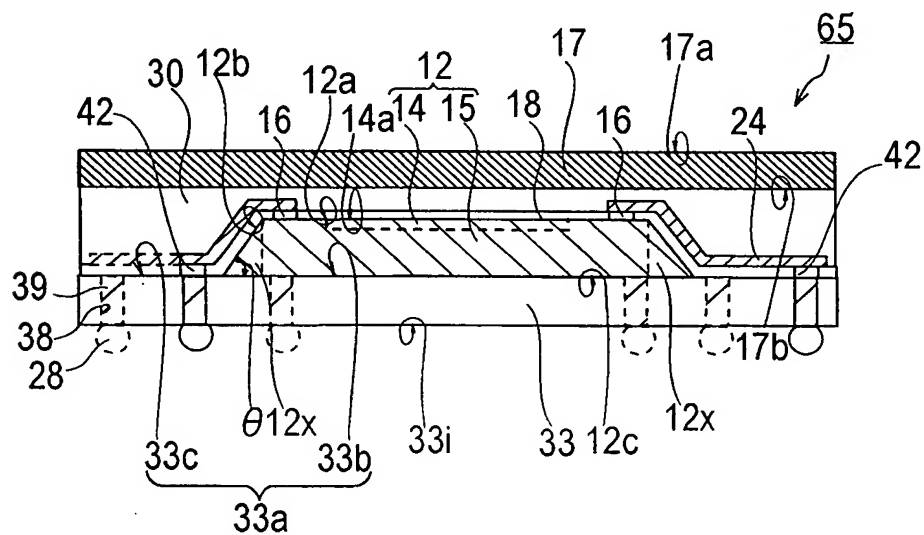


This cross-sectional view shows a semiconductor device with a central channel region 12 and side regions 12a and 12b. The channel 12 is defined by a gate stack 14 and 15, which is supported by a substrate 38. The side regions 12a and 12b are separated from the channel by spacers 16. The device includes various layers and structures, including a top layer 42, a middle layer 18, and a bottom layer 33. The bottom layer 33 is divided into regions 33a, 33b, 33c, and 33i. The side regions 12a and 12b are also divided into sub-regions 12x and 12y. The device is shown in a cross-sectional view, with the central channel 12 and side regions 12a and 12b being the primary features.

*FIG. 16*



*FIG. 17*

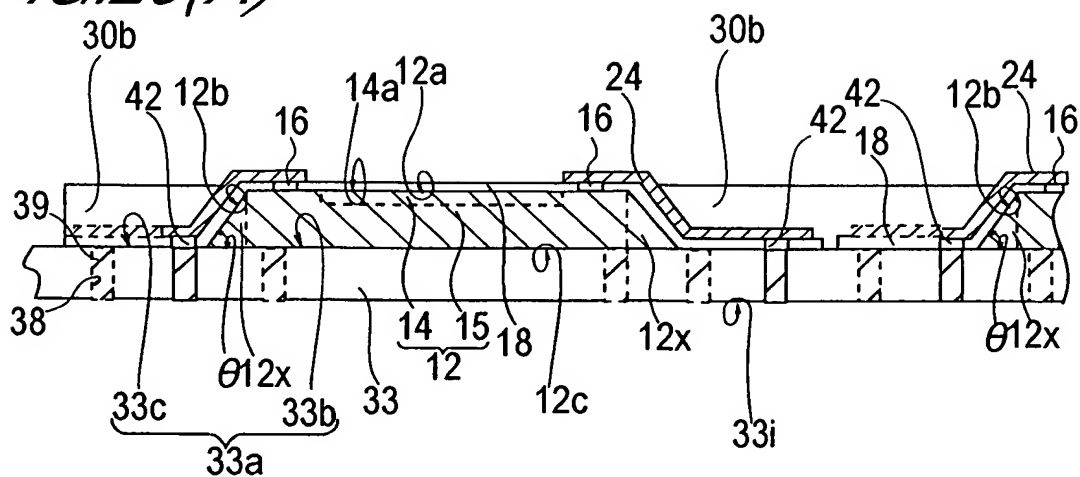




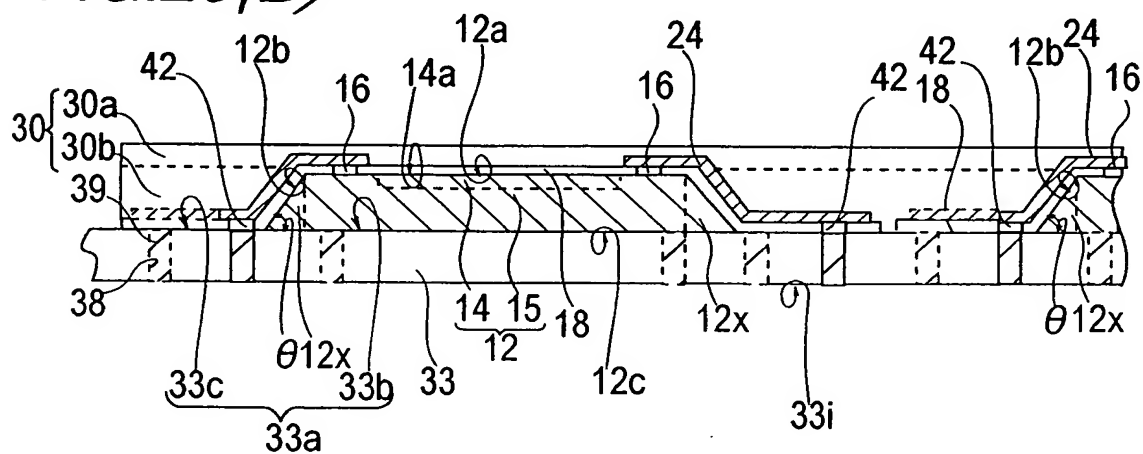
[illegible][illegible]

[illegible]

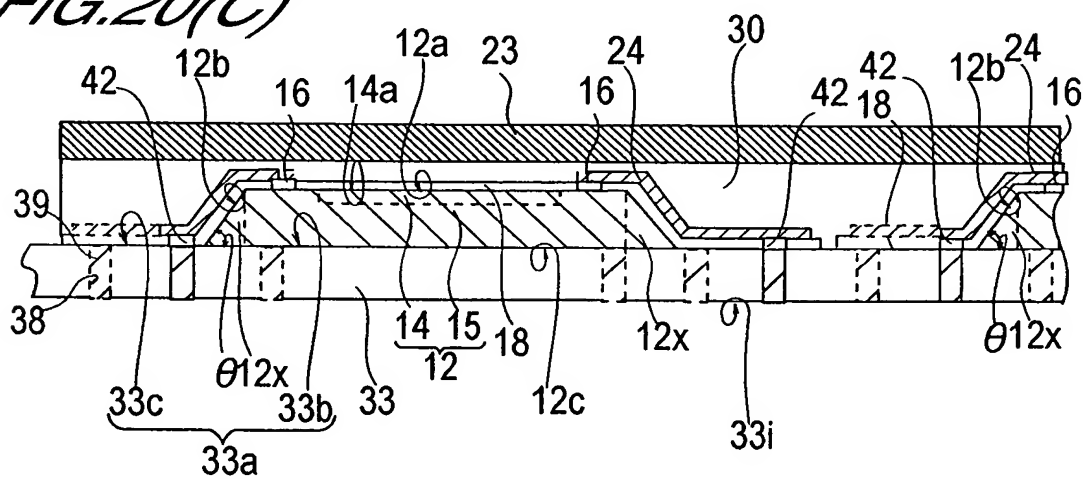
*FIG. 20(A)*



*FIG. 20(B)*



*FIG. 20(C)*





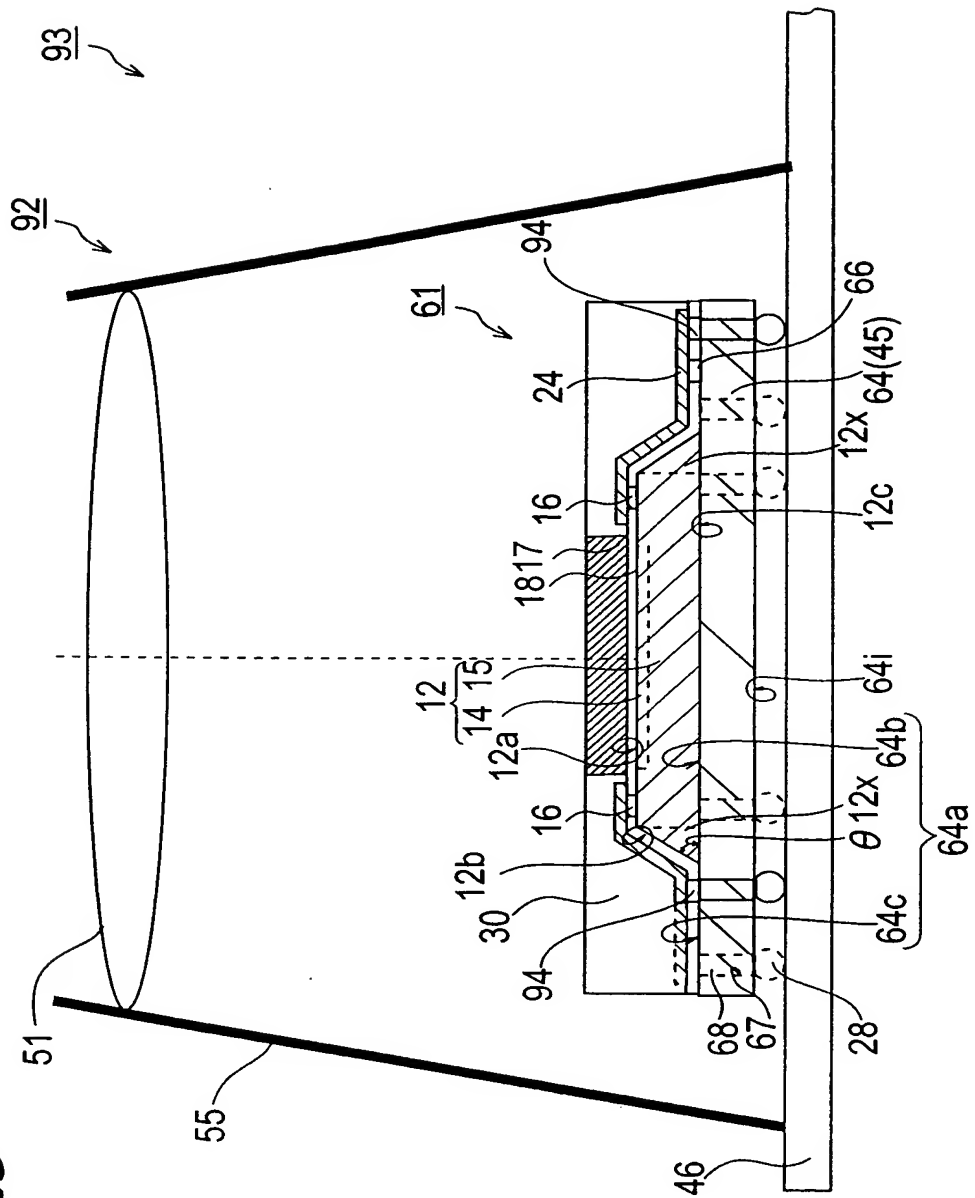
[illegible]

FIG. 24(A)

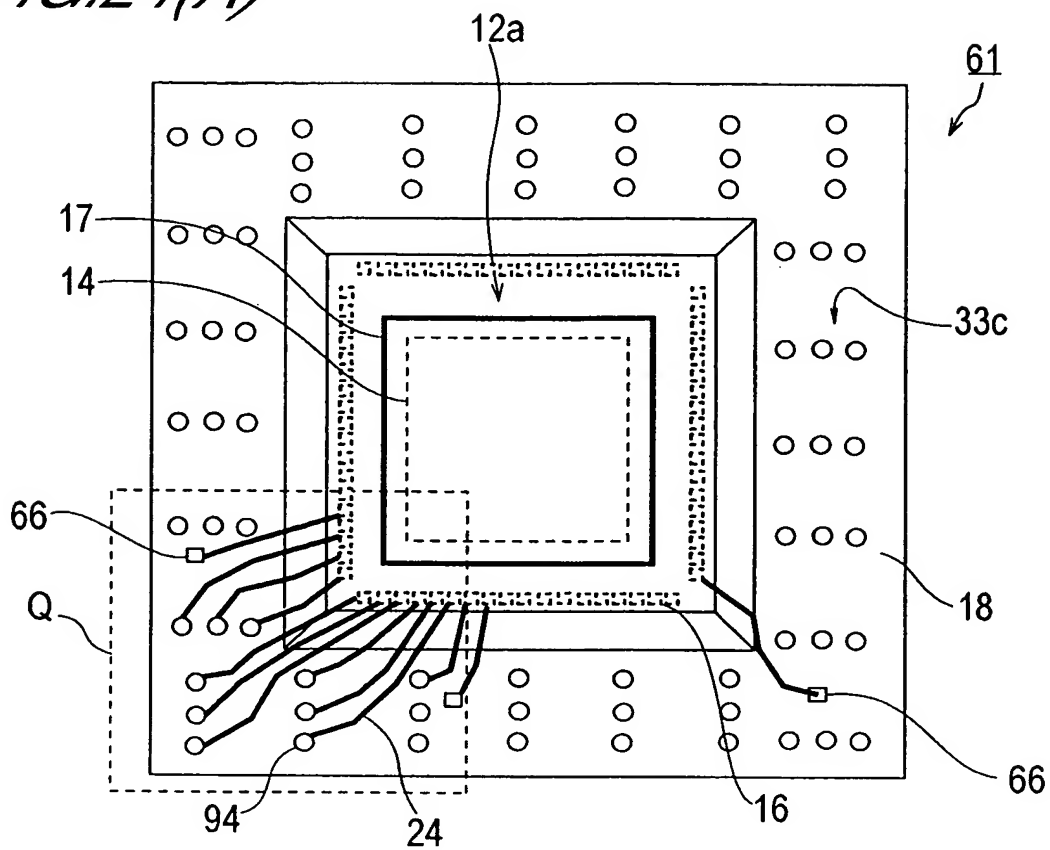
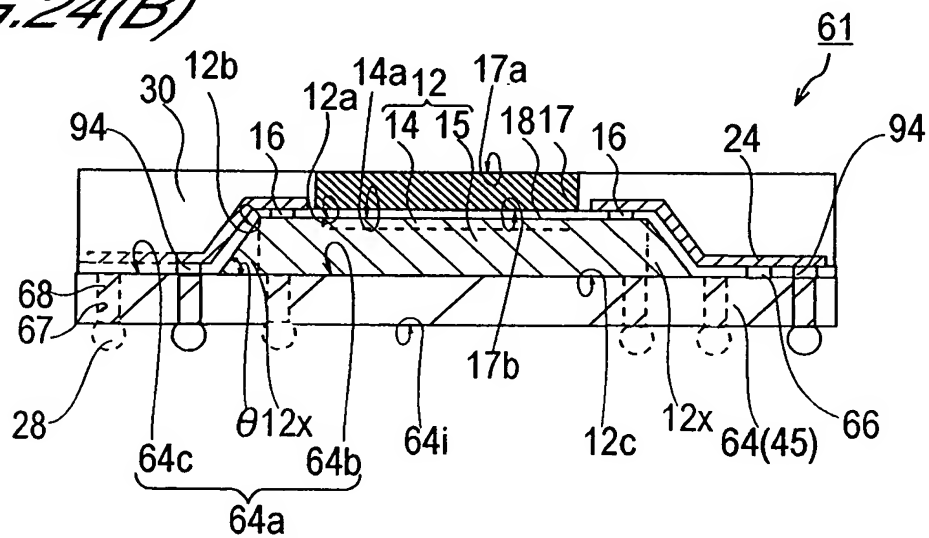


FIG. 24(B)



[illegible]

FIG. 26

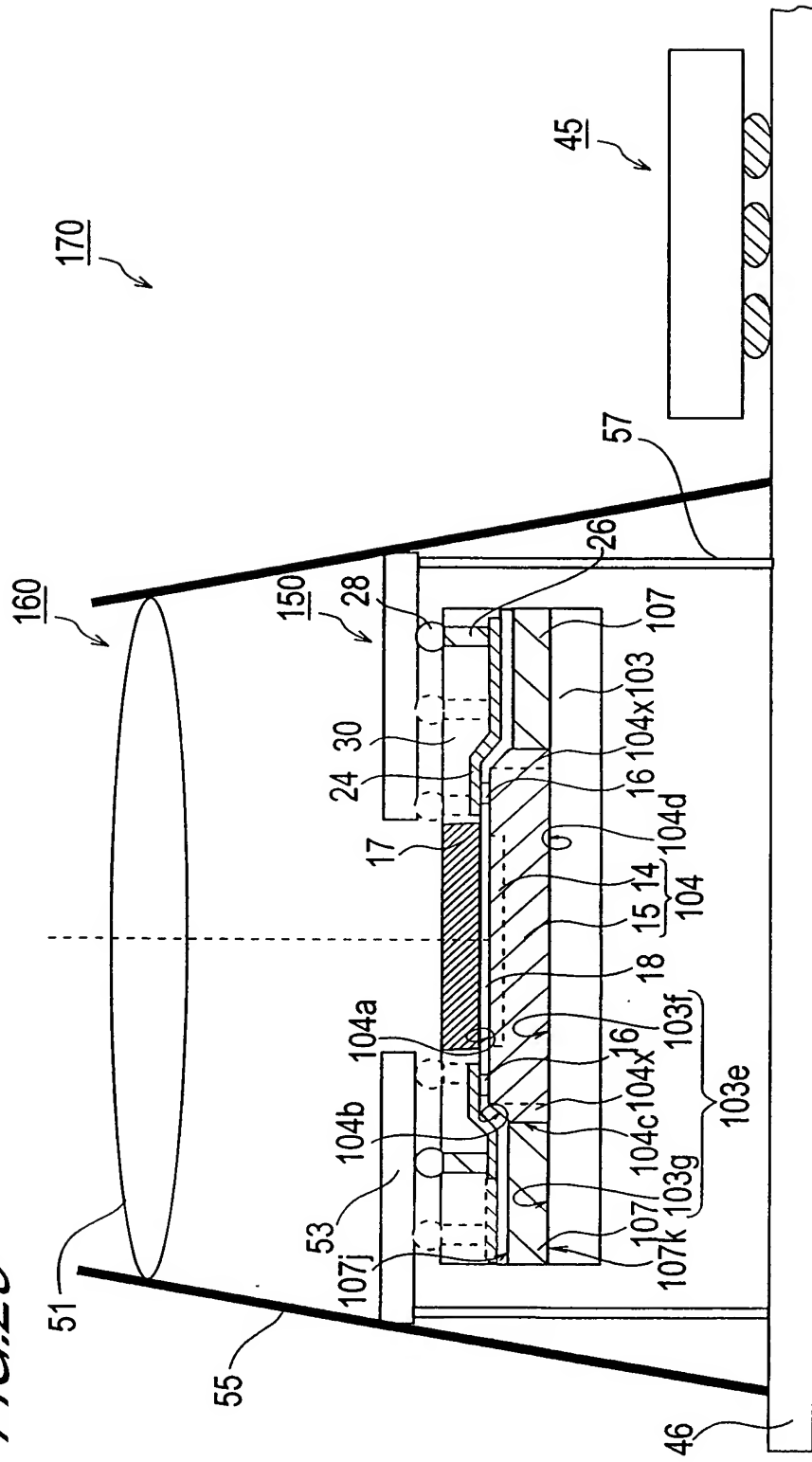




FIG. 27(A)

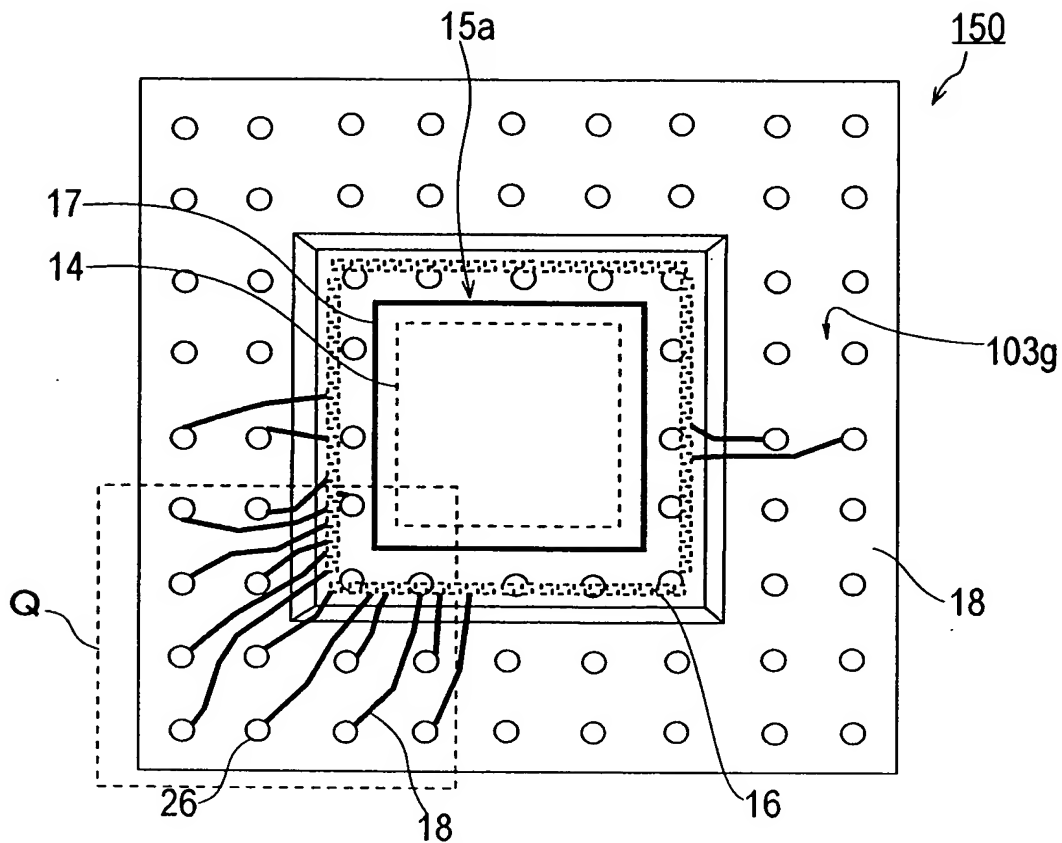
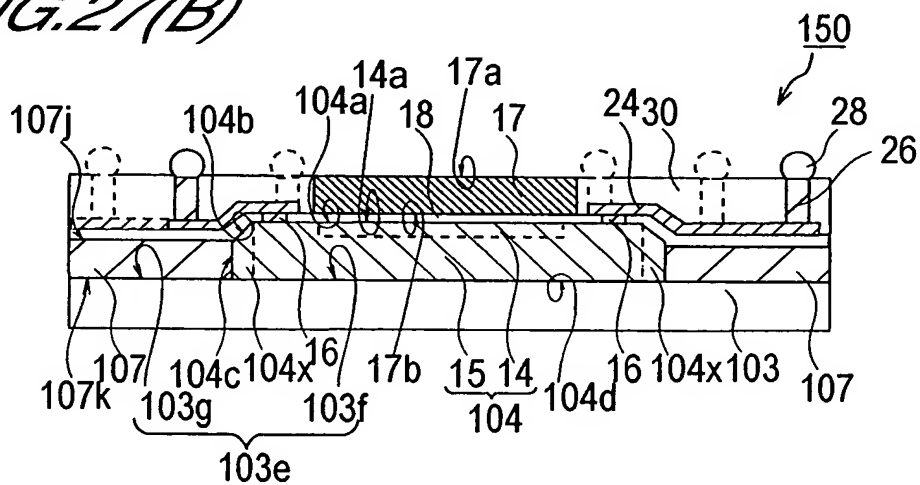
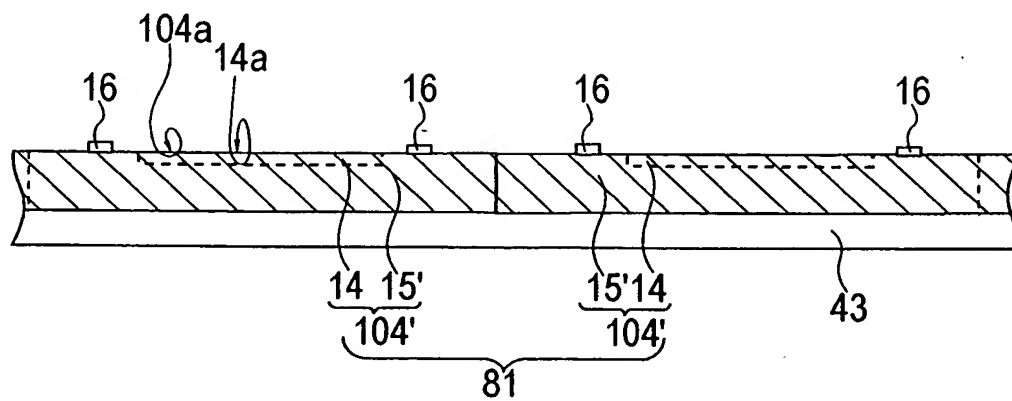


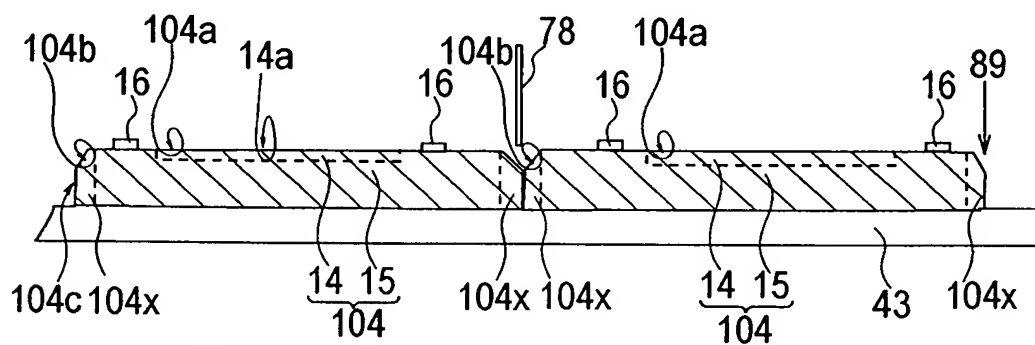
FIG. 27(B)



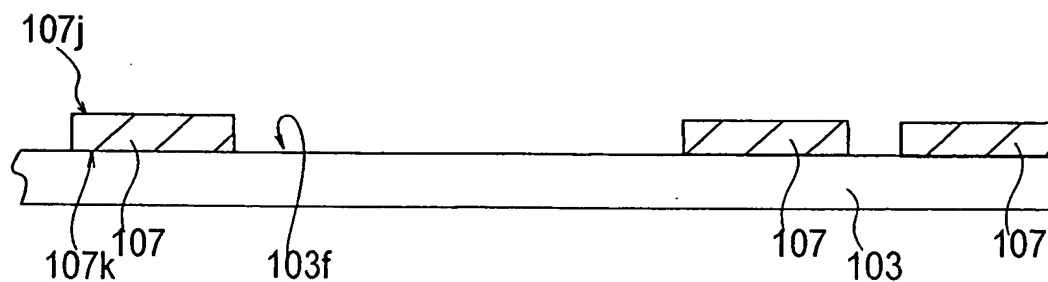
*FIG.28(A)*



*FIG.28(B)*



*FIG.28(C)*





*FIG. 30*

